



Attorney's Docket No. 1207P006D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Ting et al.

Application No.: 10/021,744

Filed: December 5, 2001

For: FLOOR PLAN FOR SCALABLE
MULTIPLE LEVEL TAB
ORIENTED INTERCONNECT
ARCHITECTURE

Assistant Commissioner for Patents
Washington, D.C. 20231

Examiner: Not Yet Assigned

Art Unit: 2154

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INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed with this document is a copy of Information Disclosure Citation Form PTO-1449. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 CFR § 1.98(d) copies of the references are not provided herein as copies of the references were provided in prior application 09/089,298 filed June 1, 1998.

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

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Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

 X 37 C.F.R. §1.97(b).

 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

 A statement pursuant to 37 C.F.R. §1.97(e) or

 A check for \$180.00 for the fee under 37 C.F.R. § 1.17(p).

 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

- (1) A statement pursuant to 37 C.F.R. §1.97(e);
- (2) A petition under 37 C.F.R. §1.97(d)(2) requesting consideration of the Information Disclosure Statement; and
- (3) A check for \$130.00 for the fee under 37 C.F.R. §1.17(i) to consider an Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

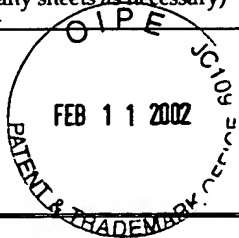
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 1207P006D	Application Number: 10/021,744
Page 1 of 5		First Named Inventor: Benjamin S. Ting	
		Filing Date: December 5, 2001	



U.S. PATENT DOCUMENTS						
Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
		4,020,469		Manning Technology Center	2100-26-77	
		4,661,901		Veneski	4-28-87	
		4,700,187		Furtek	10-13-87	
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Exam. Initial*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD- YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (If known)				
		EP	0415542 A1	A1	Advanced Micro Devices, Inc.	03/06/91		
		EP	0630115 A2	A2	Pilkington Micro-Electronics Limited	12/21/94		
		GB	2180382 A		Pilkington Micro-Electronics Limited	03/25/87		
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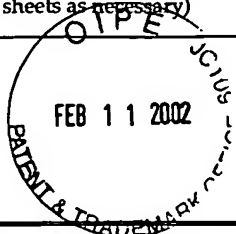
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		5,243,238		Kean	9-7-93	
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		Office ³	Number ⁴	Kind Code ⁵ (If known)				
		PCT	WO92/08286	A1	Concurrent Logic, Inc.	05/14/92		
		PCT	WO94/28475	A1	Regents of the University of California	12/08/94		
		PCT	WO96/05964	A1	Minnesota Mining and Manufacturing Company	02/29/96		
		PCT	WO96/35261	A1	BTR, Inc.	11/07/96		

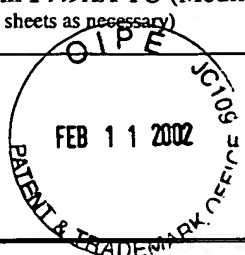
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OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		RICHARD CLIFF et al., "A Dual Granularity and Globally Interconnected Architecture for a Programmable Logic Device", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 7.3.1-7.3.5.	
		Altera Corporation, Data Sheet, "Flex EPF81188 12,000-Gate Programmable Logic Device", September 1992, Version 1.	
		MINNICK, R.C., "A Survey of Microcellular Research", Journal of the Association for Computing Machinery, Vol. 14, No. 2, April 1967, pp. 203-241.	
		SHOUP, R.G., "Programmable Cellular Logic Arrays", Ph.D dissertation, Carnegie-Mellon University, Pittsburgh, PA, March 1970 - Partial.	
		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits", UNIVAC, Division of Sperry Rand Corporation, Blue Bell, PA, Contract AF 19 (628)2907, AFCRL 66-298, Project No. 464504, November 30, 1965.	
		PING-TSUNG WANG et al., "A High Performance FPGA with Hierarchical Interconnection Structure", Institute of Electrical and Electronic Engineers, pp. 239-242, May 30, 1994.	
		Motorola Product Brief, "MPA10XX Field Programmable Gate Arrays", pp. 4 pages total, September 27, 1993.	
		KRAMBECK, R.H. "ORCA: A High Performance, Easy to Use SRAM Based Architecture", Wescon '93 record, pp. 310-320, September 20-30, 1993.	
		BUFFOLI et al., "Dynamically Reconfigurable Devices used to Implement a Self-Tuning, High Performance PID Controller », IEEE 1989, pp. 107-112.	
		DEVADAS, S., "Boolean Decomposition of Programmable Logic Arrays", IEEE 1988, pp. 2.5.1-2.5.5.	
		VIDAL, J., "Implementing Neural Nets with Programmable Logic", IEEE 1988, pp. 50-53.	

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Examiner Initials*	Cite No ¹		Translation ²
		YACHYANG SUN et al., "An Area Minimizer for Floorplans with L-Shaped Regions", 1992, Int'l. Conference on Computer Design, pp. 383-386.	
		ATMEL Corporation, "Field Programmable Gate Arrays - AT6000 Series", 1993.	
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		F. ZLOTNICK et al., "A High Performance Fine-Grained Approach to SRAM based FPGA's, Wescon '93 Record, pp. 321-326, September 28-30, 1993.	
		BARRY K. BRITTON et al., "Optimized Reconfigurable Cell Array Architecture for High Performance Field Programmable Gate Arrays", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 7.2.1-7.2.5.	
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